In the Specification

Applicant presents replacement paragraphs below indicating the changes with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

Please replace the paragraph beginning on page 9, line 16, as follows:

FIG. 32 shows a three phase clock [is a block diagram of one embodiment of a squaring circuit];

Please replace the paragraph commencing on page 13, line 25, as follows:

In one embodiment, the reference voltages V1, V3, V5 and V7 are connected to a reference voltage V_{ref} (not shown), and reference voltages V2, V4, V6, V8 are connected to ground.

Please replace the paragraph commencing on page 13, line 27, as follows:

The DAC 150 may receive a non-overlapping 3-phase clock, P1, P2, P3, shown in FIG. [3] 6. The closed/open condition of the switches S3, S6, S9, and S12 is controlled by the P3 signal of the 3-phase clock. The P1 signal of the 3-phase clock controls the open/closed condition of the charge sharing switches [[S13,]] S14, S15, and S16. The P2 signal of the 3-phase clock controls the open/closed condition of the switch S17. The logical-OR of the P1 and P2 signals, P1+P2, controls the open/closed condition of the switch S13. That is, S13 closes when either P1 or P2 is in a logical high state.

Please replace the paragraph on page 14 beginning at line 9 with the following rewritten paragraph:

FIGS. 7A-7C are block diagrams showing the operation of the SC DAC 150 of FIG. 5 for each of the 3 clock phases in the event that input terminals 172, 178, 184, and 190 are supplied with digital bit signals bit_1, bit_2, bit_3, bit_4, having logic states of 1, 0, 0, 0, respectively. Tables show the relationship between the clock phase, and the state (i.e., voltage and charge) of the capacitors in the one-bit DACs. In Fig. 7 and similarly labeled figures, the charges Q(C1)... Q(CN) represent the charge on capacitors C1... CN, respectively. Referring now to FIG. 7A, on phase P3 of the 3-phase clock, all of the charge sharing switches S13, S14, S15, and S16 and the output switch S17, are in the open condition. The capacitor C1 is charged to V_{ref} in response to the logic state 1 on terminal 172. Capacitors C2, C3 and C4 are all discharged to ground in response to the logic state 0 signals on terminals 178, 184, 190, respectively. Referring now to FIG. 7B, on phase P1 of the 3-phase clock, all of the charging switches S3, S6, S9 and S12 (FIG. 5) and the output switch S17 are in an open condition, and all of the charge sharing switches S13, S14, S15 and S16 are in a closed condition, whereby charge is redistributed and resulting in the total charge on all of the capacitors being divided among all of the capacitors. If the capacitors C1, C2, C3, C4 all have the same capacitance value C, then the charge is shared equally so that the voltage across each capacitor becomes $V_{ref}/4$. Referring now to FIG. 7C, on phase P2, charge sharing switches S14, S15, and S16 are in the open condition, output switch S17 is in the closed condition, and capacitor C1 (FIG. 5) of one-bit DAC 162 delivers its charge to the output terminal 160. On the next occurrence of phase P3 (not shown), the multi-bit digital signal bit_1, bit_2, bit_3, and bit_4 may be updated and provided to the DAC 150 via input terminals 172, 178, 184, 190.--

Please replace the paragraph commencing on page 17, at line 6, as follows:

Referring now to FIG. 10, in another embodiment, the SC DAC 150 described with respect to FIGS. 7A-7C operates with a non-overlapping four-phase clock, e.g., the four-phase clock illustrated in FIG. 9 instead of the ~~three-phase~~ three-phase clock of FIG. 6. On phase P3 of the ~~four-phase~~ four-phase clock, the condition of the SC DAC 150 is the same as that described above with respect to FIG. 7A. On phase P4 of the ~~four-phase~~ four-phase clock, the condition of the SC DAC 150 is the same as that described above with respect to FIG. 7B. On phase P1 of the ~~four-phase~~ four-phase clock, the condition of the SC DAC 150 is the same as that described above with respect to FIG. 7C. FIG. 10 shows the state of the SC DAC 150 on phase P2 of the ~~four-phase~~ four-phase clock. On phase P2 of the ~~four-phase~~ four-phase clock, the charging switches S3, S6, S12 (FIG. 5) are in the open condition, ~~charge-sharing~~ charge-sharing switches S13, S15, S16 are in the open condition, and switch S14 and output switch [[S19]] S17 are in the closed condition, wherein C2 of the one-bit DAC delivers its charge to the output terminal 160. Thus, in such embodiment, two copies, each indicative of the sum of the values of the bits in the multi-bit digital input signal, are separately delivered to the output terminal. As described above, in this embodiment, they are delivered one after the other. However, in another embodiment, they may be delivered simultaneously.

Please replace the paragraph of page 25 beginning at line 17 with the following rewritten paragraph:

FIG. 24 is a block diagram of one embodiment of a ~~four-bit~~ four-bit scrambler 400 that receives a ~~three-bit~~ three-bit digital input signal, bit_A, bit_B, bit_C, represented by the labeled arrows on the left, and outputs scrambled bits, represented by the arrows on the right. A scrambler is typically most effective when all of the scrambler inputs receive data . The extra input(s) of the scrambler may for example be "hardwired" to a logic state, i.e., a 1 or a 0. In this event that an input(s) of a scrambler is hardwired, it may be desirable to hardwire a corresponding number of DAC input(s), to a logic state opposite to that used for the extra input(s) of the scrambler.--

Please replace the paragraph commencing on page 29, line 27, as follows:

FIG. 28A is an illustration of a top view of one embodiment of a SC cell 450 implementing the one-bit DAC of FIG. 16A. The perimeter of the SC cell 450 is shown as a dotted line. The SC cell 450 includes a capacitor top plate C1TP and a capacitor bottom plate C1BP. A conductor 452 is provided to supply the digital signal bit_2 to a region of a control portion 222. A conductor 454 is provided to supply the phase signal [[P2]] P3 to a region representing a control portion 222. A conductor 456 runs from the perimeter of the SC cell 450 to a gate of a switch S43. A conductor 458 runs from the perimeter of the SC cell 450 to one of a source or a drain of the switch S43. A conductor 460 runs from the perimeter of the SC cell 450 to the top plate of the capacitor C1TP and to the other of the source or drain of the switch S43. A conductor 462 runs from the perimeter to one of a source or a drain of a switch S48. A conductor 464 runs from the other of the source or drain of the switch S48 to the top plate of the capacitor C1TP and to a region 466 representing a region of a switch S4, a switch S5, voltage reference V3, and voltage reference V4. A conductor 468 runs from a gate of the switch S48 to the perimeter of the SC cell 450.

In the Drawings

A Request for Approval of Proposed Drawing Corrections is enclosed along with revised Fig. 10 and a copy of original Fig. 13, showing changes in red.

With respect to Fig. 10, a drawing correction is being made herewith with respect to the label on the output switch, which should have been S17, not S19. In Fig. 13, reference numeral 152 is being deleted.